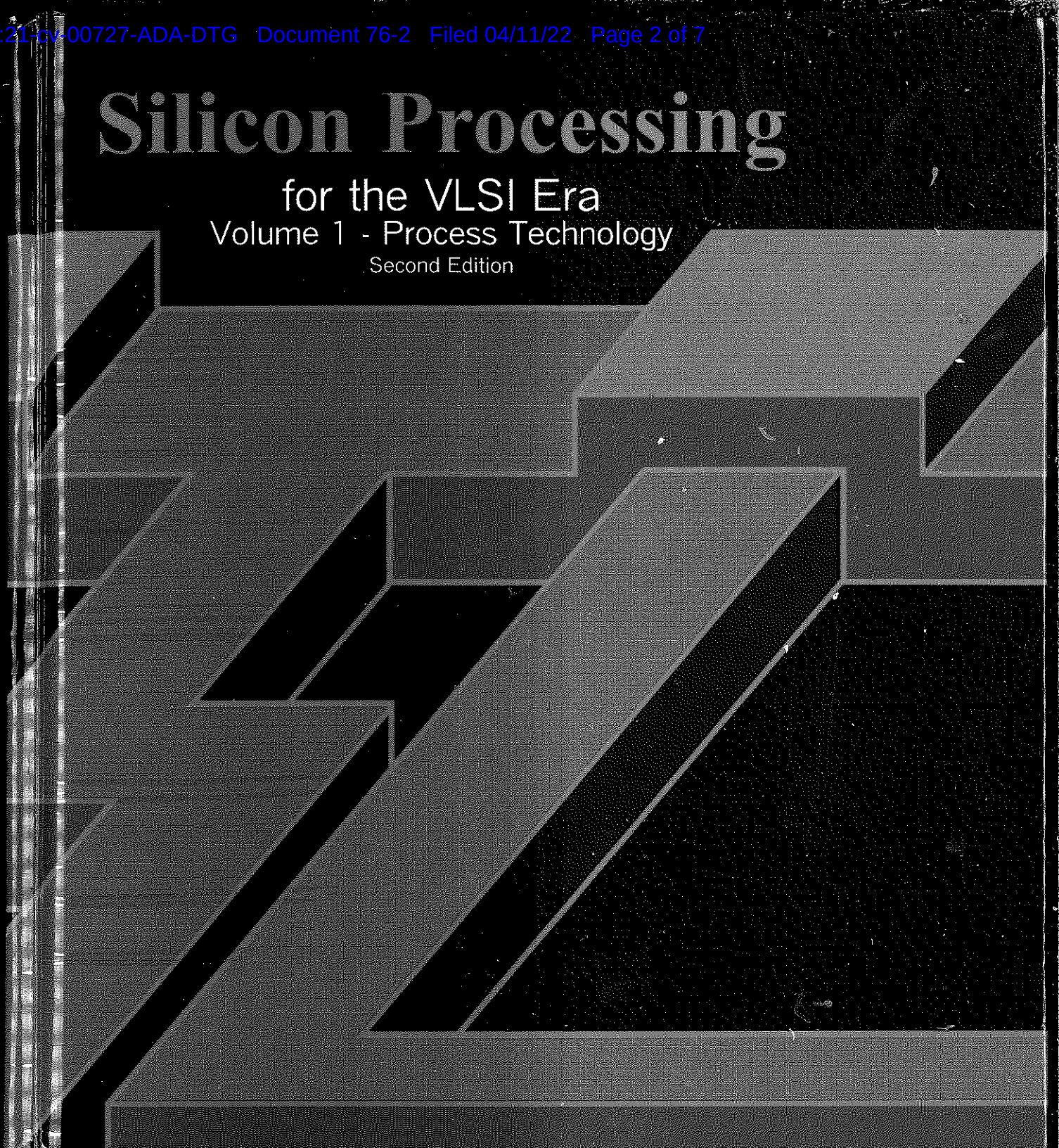
EXHIBIT A

Silicon Processing

for the VLSI Era

Volume 1 - Process Technology

Second Edition



SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

Second Edition

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keypad, and many stations include host computer interfacing capabilities for processing and storing this data.[65]

In more automated systems, the human operator is completely removed from the *defect inspection task. In-process wafer inspection systems*, based on automatic image processing have been introduced. Defect detection is accomplished either by die-to-die or die-to-database comparison. Manufacturers of these systems claim defect detection sensitivities well into the sub-micron range. Such instruments, however, often have difficulty detecting particles on substrates that have surface granularity, or particles on wafers containing surface topography. In addition, for particles near the minimum-size detection limit, such machines can miss the presence of some particles, and signal the detection of others that may be non-existent.

The remainder of this section discusses linewidth measurement techniques used to verify that critical dimensions have been produced. Procedures are described for monitoring the variation of linewidths produced in a production environment as a function of time. Such data can serve as a gauge for tracking the performance of a lithographic process line.

12.4.7.1 Linewidth Variation and Control: There are two aspects of feature sizes that must be controlled in the lithographic/etching process: 1) the absolute size of a minimum feature, including linewidth, spacing, or contact dimensions (also referred to as a *critical dimension*, or CD), and 2) the variations of the minimum feature sizes as they cross steps on wafer surfaces. Linewidth (and spacing) measurements are regularly performed to determine the actual sizes of CDs at each masking level of a process. The variation of linewidths over steps are also monitored (causes of the variation were discussed in the section on *Resist Processing: Exposure*). These two aspects are mentioned together because a tradeoff exists between absolute linewidth size and variation of the size over steps. Over-exposure and over-development can improve linewidth control, but at the expense of linewidth size. Figure 12-36 shows a SAMPLE simulation which calculates linewidth variation ΔL across a 0.5 μm step, as the line sizes vary with changing exposure and development. It shows that linewidth variation over steps can be considerably reduced by over-exposure, but at the expense of dimensional accuracy.[64]

Another issue involving linewidth control is that correct feature *sizes* must be maintained across an entire wafer, and from one wafer to another. The ability to do this is referred to as *linewidth control*. As feature size is reduced, the tolerable error on feature size control is also

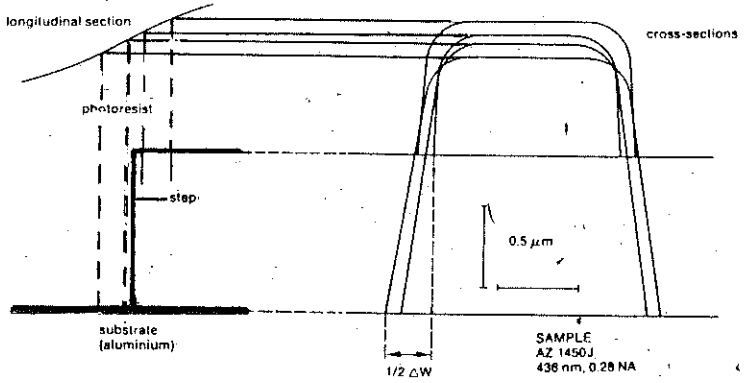

Fig. 12-36 Longitudinal section and cross sections of a photoresist line running across a one micron aluminum step. The resist profiles are simulated by SAMPLE. The nominal linewidth is 1.8 μm.[64] Reprinted with permission of SPIE.

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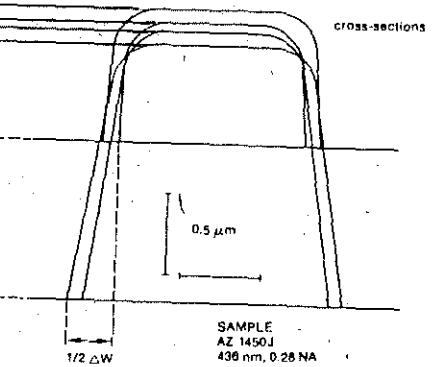

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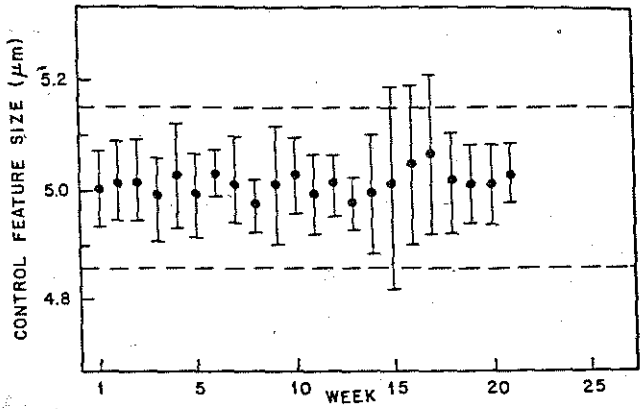

Fig. 12-37 Linewidth control data for a typical process line. Weekly averages are shown for a 5.0 μm control feature. The dashed lines represent limits. Note weeks 15-17 represent a processing problem that was corrected in week 18. Reprinted from Ref. 8 with permission of the American Chemical Soc.

decreased. For example, the required tolerance on a nominal 1-μm linewidth of polysilicon features is typically ± 10%, or ± 0.1 μm. Note that when exposure is performed by a wafer stepper, feature size must be controlled across *every exposure field*, and *field-to-field* variations in feature sizes must also not exceed acceptable limits.

Linewidth control is impacted by a variety of factors, depending on hardware, processes, and materials. The degree of control is determined by measuring a series of test structures with known feature sizes across a wafer, and then plotting the feature dimension as a function of location on the wafer. The standard deviation at the one and two sigma level then becomes a measure of the linewidth control capability of a particular exposure/resist process. For example, in a process that has minimum linewidths of 0.35 μm, and spaces of 0.35 μm, the controllability specification might be a maximum 10% linewidth variation, with 95% (2σ) confidence. Such data are then plotted as a function of time (Fig. 12-37) and are utilized to monitor the performance of a lithographic line.

12.4.7.2 Linewidth Measurements: The width of features produced on wafers are measured in many phases of the fabrication process, including: a) after development; b) after etching; and c) during photomask production. A number of techniques are currently utilized to perform such feature size measurements. For ULSI applications the measurement technique must be repeatable to less than 0.1 μm in order to verify that the ±10% size tolerance specification (cited as an example in the previous section) is satisfied during fabrication. In fact, it is argued that the measurement uncertainty of the metrology system must even be smaller. That is, in the 1 μm polysilicon line described above, if the uncertainty in the etching process is ± 0.03 μm, then it must be necessary to determine that its photoresist linewidth is 1 μm ± 0.07 μm.[66] The National Bureau of Standards (NBS) is involved in developing linewidth measurement standards that can be used to calibrate commonly used linewidth measurement equipment.[67] Calibration standards for photomasks have been available for some time from the NBS and are in widespread use. They were the first to be developed because line edges on masks are well defined, and good contrast exists between light transmitted through the mask and opaque feature edges. Measurement on processed wafers are much more complicated, and the NBS has not yet released such

standards. Calibration by semiconductor manufacturers is commonly made to a known "good" wafer, which is then used as the standard. Most linewidth measurement systems employ either visible-light optics, He-Ne laser light, or electron-beam optical techniques.[69] Current optical techniques based on ordinary microscopes are satisfactory for use with 1.0 μm (or larger) feature sizes. These systems will continue to find wide applicability because of their low cost, ease of use, and high throughput. Future development will be directed at improving these attributes while maintaining the required accuracy and precision. For smaller geometries, SEM and laser scanning techniques are more frequently employed.

Measurement of linewidth by optical techniques is accomplished with the following types of systems: a) mechanically scanning an optical slit across the magnified feature image; b) video scanning across the feature of interest; c) image shearing; and d) scanning a laser spot across the feature, and detecting the reflected image. In the *scanning slit technique* (Fig. 12-38), the light passing through the slit is measured by a photomultiplier tube (PMT) to form a micro-densitometer profile, which is then used to perform the linewidth measurements. The operator views the image through a binocular microscope or color crt. The narrow slit (e.g., 200 nm wide) is moved across the image (e.g., in 25 nm increments), and the intensity profile is acquired via the PMT. The profile is then analyzed by an edge-sensing algorithm to determine the dimension. An auto-focus algorithm can also be used to find the "best" focus, by moving the motorized stage in the z-axis until the maximum slope of the selected edge is located (or, in some systems, by use of an independent laser focus technique). In *video based systems*, a video camera is used to capture and store the profile of the feature of interest (Fig. 12-39). An operator

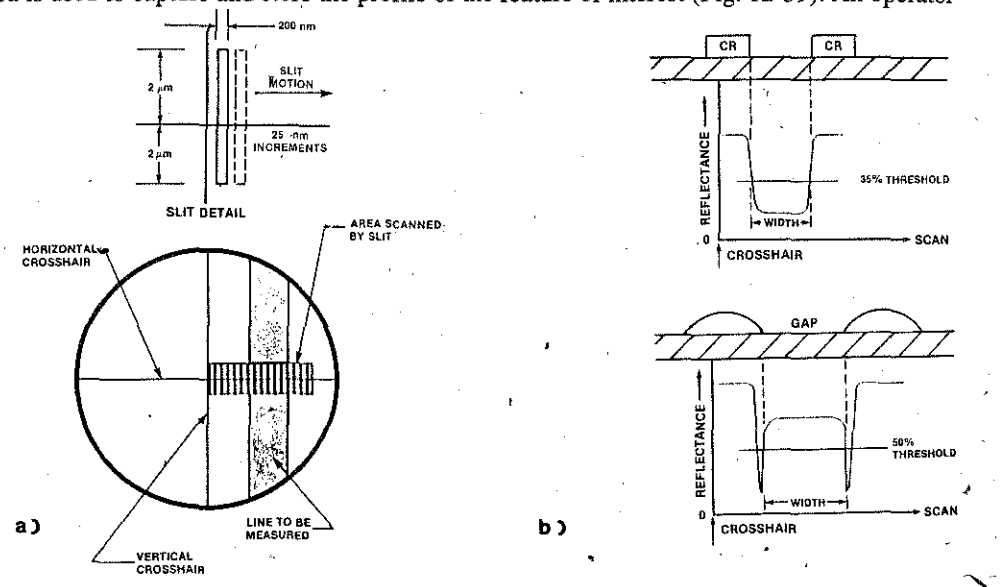

Fig. 12-38 a) The slit scan technique utilizes an image profile by analyzing the data obtained by scanning a slit across the wafer.[68] Reprinted with permission of Semiconductor International. b) When viewed through the binocular, the crosshair and line to be measured are superimposed. An open field is placed at the vertical crosshair, with the line of interest to the right on the horizontal crosshair. The 200-nm-wide by 4 μm wide slit then scans a path 4 μm wide by 10 μm long in 25 nm increments.[69] Reprinted by permission, Microelectronics Manufacturing and Testing.